Remarks

The non-final Office Action dated April 29, 2010, withdrew the application from appeal, indicated that claims 4, 6, and 14 are objected to but would be allowable if rewritten in independent form, and listed the following new grounds of rejection: claims 1-3, 5, 7-10, 12 and 15 stand rejected under 35 U.S.C. § 103(a) over Brokaw (U.S. Patent No. 6,040,732) in view of Huijsing *et al.* (U.S. Patent No. 4,555,673); claim 2 stands rejected under 35 U.S.C. § 103(a) over the '732 reference in view of the '673 reference and Nishimura (U.S. Patent Pub. 2001/0004255); claim 13 stands rejected under 35 U.S.C. § 103(a) over the '732 and '673 references in view of Miyazawa *et al.* (U.S. Patent Pub. 2002/0196247); and claim 11 stands rejected under 35 U.S.C. § 103(a) over the '732 reference in view of the '673 reference and Applicant's Admitted Prior Art (AAPA). In this discussion set forth below, Applicant traverses each rejection without acquiescing to any averment in this Office Action unless Applicant expressly indicates otherwise.[1]

Each of the § 103(a) rejections fails because the Office Action does not attempt to assert the cited combinations of references as purporting to have correspondence. For example, the Office Action does not assert that the references teach the claimed invention "as a whole" (§ 103(a)) including, *e.g.,* keeping the ratio of the transconductance of a NMOS transistor doublet and the transconductance of a PMOS transistor doublet constant. Because none of the cited references are represented as teaching these aspects, no reasonable combination of these references can provide correspondence. As such, the § 103 rejection fails.

More specifically, the '673 reference is asserted as teaching constant transconductance, but the Office Action does not attempt to equate this general teaching implicitly or otherwise, with any relevant ratio. Moreover, Applicant fails to recognize how the '673 reference would teach keeping the transconductance of differential input portions 20 and 22 (*i.e.*, the asserted NMOST and PMOST doublets) at a particular ratio, as it appears to teach controlling the transconductance of the differential amplifier that includes the differential input portions 20 and 22. *See, e.g.*, Figure 2. The '673 reference

[1] Applicant notes a typographical error at line 1 in each of paragraphs 2 and 3, erroneously listing claims 4, 6, and 14.

discusses controlling the transconductance of the differential amplifier to be largely constant, and does not expressly teach or mention the transconductance of differential input portions 20 and 22 being relative to each other (*i.e.*, the ratio of their transconductances). *See, e.g.,* Abstract and Col. 2:40-49. As the Office Action acknowledges that the '732 reference does not teach a transconductance ratio (Office Action page 3), the § 103(a) rejections lack correspondence and are improper.

The Office Action's inability to assert such correspondence may be related to the lack of motivation to combine the references as asserted. For example, the cited references teach away from the Office Action's proposed combination. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('732) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). Applicant submits that the combination would render the invention inoperable because the asserted hypothetical embodiment replaces two doublets having the same channel type with two doublets having different channel types. The circuit of the '732 reference would not be able to provide the proper voltage levels to the NMOS doublet, and the NMOS doublet would not function properly without a complete rearrangement of the switches within the '732 reference circuit. Under M.P.E.P. § 2143.01, the rejections cannot be maintained.

The Office Action also fails to provide a proper motivation for the proposed combination of references. Under M.P.E.P. § 2143, the Office Action must provide some articulated reason as to why one of skill in the art would have pursued the proposed modification. In the instant case, the Office Action attempts to assert that the proposed modification would be "obvious to try." However, the Office Action provides an unsupported assertion that the change from two PNP transistor doublets to an NMOS transistor doublet and a PMOS transistor doublet would reduce power consumption. While MOSFET are generally known to have low power consumption, this does not explain why one of skill in the art would change the channel type of one of the transistors

instead of simply replacing all the PNP transistors with PMOS transistors. The Office Action has not provided an explanation as to why one would modify a system designed around doublets having the same channel type, to doublets having different channel types. Thus, the Office Action has failed to provide a proper motivation for the asserted modification to the primary reference. Accordingly, the § 103(a) rejection is improper and should be withdrawn.

The Office Action also mistakenly interprets the teachings of the '732 reference with regards to Figure 5, at Col. 6:46-Col. 76:44, *see* Office Action page 2-3. The '732 reference citation expressly teaches that the circuit, and asserted transistors Q4 and Q21, use a series of switches to isolate the input node of the doublet that is disabled. *See, e.g.,* the '732 reference Col. 7:31-44. The '732 reference makes no mention of providing the analog input to only one of the two inputs. In addition, the '732 reference does not appear to expressly teach applying a reference voltage to the input of the doublet that is disabled. Rather, it appears that instead of changing the input provided to the differential input of the doublet, the switches simply isolate one of the doublets from the rest of the circuitry if desired. Accordingly, the '732 reference fails to correspond to the claimed invention and the § 103(a) rejection should be removed.

The impropriety of the § 103(a) rejections is further illustrated by the rejection of claim 3. The Office Action's rejection acknowledges that the hypothetical combination lacks correspondence to certain aspects of claim 3, and then attempts to assert that the '732 reference corresponds to these aspects simply because "these inputs are connectable to switches if one decides to place a switch there," Office Action, page 4. However, the Office Action provides no motivation to place a switch there other than Applicant's specification and claims. To say that a claim is anticipated or obvious based on such an assertion, without support, amounts to improper hindsight reconstruction. Further, the rejection fails to consider the numerous modifications to the circuit required to operate the switches once placed between the input and the gate. The switches must be provided some signal to function, and the circuitry to provide said signal is not present in the primary '732 reference. Moreover, such a basis for rejection is tantamount to saying that any modification to a reference is obvious as long as one decides to make the

modification. Accordingly, the asserted hypothetical embodiment lacks correspondence, and the § 103(a) rejection of claim 3 is improper and should be removed.

Applicant has made a grammatical correction to claim 1. This amendment is not made for the purpose of patentability.

Applicant has amended claim 14 to incorporate the limitations of claim 1. Accordingly, Applicant believes claim 14 to be in condition for allowance.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the attorney/agent overseeing the application file, David Schaeffer, of NXP Corporation at (212) 876-6170 (or the undersigned).

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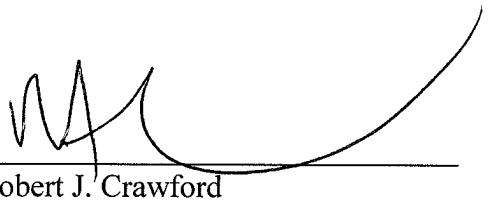
By: 

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